REMARKS/ARGUMENTS

In the Office action dated June 30, 2004, the Examiner objected to claims 1, 5, 10, 11, 16, 17 and 20 because of informalities. Claims 1, 10, and 16 were objected to because of the manner of Applicants' use of the term "shallow trench isolation." Claim 11 was objected to because of the use of a relative term, which also appears in claim 17. Claims 5, 11, and 17 were objected to because of the description of multiple oxide layers in the structure of the method of the invention. Claim 20 was objected to because of an erroneous claim dependency.

In the Specification, page 4 is amended to correct a typographical error.

In the Claims, claims 1, 5, 10, 11, 16, 17 and 20 are amended.

In response to the Examiner's request, claims 1 and 5 are presented below with reference numbers from the Specification and drawings inserted therein. Such numbering also applies to similar language presented in claims 9, 10, 15, 16 and 17.

Claim 1

A method of forming an H_2 passivation layer in a FeRAM, comprising:
preparing a silicon substrate, including doping to form a P-type silicon wafer, including threshold adjustment ion implantation, shallow trench isolation (12), growth of a gate oxide (14), deposition of a polysilicon layer (16), ion implantation to form an N^+ source (18) and an drain (20); smoothing the oxide (14) by CMP, and patterning and etching the polysilicon layer (16) (described in Specification, page 3, line 4 to page 4, line 11);
depositing a layer of TiO_x (28) thin film, where $0<x<2$, on a damascene structure;
plasma space etching of the TiO_x thin film to form a TiO_x sidewall;
annealing the TiO_x side wall thin film to form a TiO_2 thin film;
depositing a layer of ferroelectric material (30); and
metallizing (36) to form a FeRAM.

Claim 5

The method of claim 1 which includes, after said preparing, depositing a layer of oxide (no reference number *per se*, however, this is a part of element 24 in Fig. 2); smoothing the oxide by CMP; stopping at the level of the polysilicon layer (16); depositing a bottom electrode (22); depositing another layer of oxide (24) by CVD; smoothing the other layer of oxide (24) by CMP, stopping said smoothing at the level of the bottom electrode; depositing yet another layer of oxide (26) by CVD; and patterning and etching the oxide layers (24, 26) to form trench structures.

It is believed that the foregoing should clarify the arrangement of the various oxide layers.

With respect to claims 11 and 17, the "larger size" language has been removed.

With respect to claims 1, 10 and 16, the additional description following "shallow trench isolation" has been removed.

Claim 20 has been amended to correct dependency.

In light of the foregoing amendment and remarks, the Examiner is respectfully requested to reconsider the rejections and objections stated in the Office action, and pass the application to allowance. If the Examiner has any questions regarding the amendment or remarks, the Examiner is invited to contact the undersigned.

Provisional Request for Extension of time in Which to Respond

Should this response be deemed to be untimely, Applicants hereby request an extension of time under 37 C.F.R. § 1.136. The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any over-payment to Account No. 19-1457.

Respectfully submitted,

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David C. Ripma
Registration No. 27,672

David C. Ripma
Patent Counsel
Sharp Laboratories of America, Inc.
5750 N.W. Pacific Rim Highway
Camas, WA 98607

Telephone: (360) 834-8754
Facsimile: (360) 817-8505